ABSTRACT OF THE DISCLOSURE

An apparatus for detecting erroneous speculative branches made by a pipelined microprocessor and for correcting the erroneous branches. A branch target address cache (BTAC) caches target addresses of executed branch instructions. A speculative branch is performed to a cached target address early in the pipeline based on a hit in the BTAC of an instruction cache fetch address before the instruction is decoded. When the speculative branch is performed, a hit bit is set. Later in the pipeline, the presumed branch instruction is decoded and executed. If the hit bit is set for the instruction, the decoded instruction is examined and the correct target address and direction are compared to the speculative versions to determine if an error was made by speculatively branching. If an error is detected, the branch target address cache is updated or invalidated, and the processor branches to the appropriate address to correct the error.